FLYING TAIL TYPE RIGID-FLEXIBLE PRINTED CIRCUIT BOARD

[0001] This application is a Continuation of U.S. patent application Ser. No. 13/771,830 filed on Feb. 20, 2013, which claims benefit under 35 U.S.C. §119(a) of Korean Patent Application No. 10-2012-0017509 filed Feb. 21, 2012, in the Korean Intellectual Property Office, the contents of all of which are incorporated herein by reference in their entireties.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to a method of manufacturing a flying tail type rigid-flexible printed circuit board and a flying tail type rigid-flexible printed circuit board manufactured by the same, and more particularly, to a method of manufacturing a flying tail type rigid-flexible printed circuit board using a flexible insulator and a flying tail type rigid-flexible printed circuit board manufactured by the same.

[0004] 2. Description of the Related Art

[0005] In recent times, as the degree of integration of semiconductor elements is gradually increasing, the number of pads provided on the semiconductor elements to connect the semiconductor elements to external circuits is increasing and mounting density is also on an increasing trend. For example, when a minimum processing dimension of the semiconductor element made of silicon is about 0.2 μm, it is required to provide about 1000 pads on the semiconductor element with a size of about 10 mm.

[0006] Further, in semiconductor devices such as semiconductor packages, on which the semiconductor elements are mounted, miniaturization and thinning are needed to improve the mounting density, and particularly, in order to respond to portable information devices such as notebook personal computers (PCs), PDAs, and mobile phones, miniaturization and thinning of the semiconductor packages are needed.

[0007] In order to package the semiconductor element, it is required to connect the pad of the semiconductor element to a pad of a wiring substrate as well as mounting the semiconductor element on the wiring substrate. However, when about 1000 pads are provided around the semiconductor element with a size of about 10 mm, they are provided with a very fine pitch of about 40 μm. In order to connect the pads provided with a fine pitch to the pad provided on the wiring substrate, since very high accuracy is required for wiring on the wiring substrate or positioning upon connection, it is very difficult to apply a conventional wire bonding or tape automated bonding (TAB) technique.

[0008] Accordingly, recently, various multilayer printed circuit boards, which can mount electronic components on surfaces thereof, have been developed according to miniaturization and integration of the electronic components, and particularly, active researches on a flying tail type rigid-flexible printed circuit board, which can minimize a space occupied by a printed circuit board and be three-dimensionally and spatially transformed, are in progress.

[0009] This flying tail type rigid-flexible printed circuit board, which consists of a rigid domain (hereinafter, R) having mechanical strength due to an embedded insulating layer and a flexible domain (hereinafter, F) that connects the rigid domains R to each other and has elasticity, is mainly used in small terminals, such as mobile phones, requiring high integration by removing an unnecessary space due to use of a connector in response to demands for high integration and fine pitches of mounted components according to high functionality of mobile devices.

[0010] When looking into a conventional method of manufacturing a flying tail type rigid-flexible printed circuit board, first, a first inner circuit pattern layer is formed on one or both surfaces of a base substrate, and a coverlay is attached to the inner layer circuit pattern layer of a flexible domain F (step **S1**).

[0011] Next, a first insulating layer is laminated on a rigid domain R, and a first metal layer is laminated on the first insulating layer including the flexible domain F (step **82**).

[0012] At this time, it is preferred that the first insulating layer is made of a cured insulator so that the first insulating layer is not laminated on the flexible domain F. Since the first metal layer is laminated on the first insulating layer and the first insulating layer is not laminated on the flexible domain F, the first metal layer is formed not to be in contact with the coverlay.

[0013] Next, a first window is processed by removing the first metal layer in a blind via-hole forming domain, which is to be formed in the rigid domain R (step **83**).

[0014] Next, a blind via-hole is processed by processing the first insulating layer, which is exposed by the first window, with C02 laser (step **84**).

[0015] Next, a through-hole, which penetrates the entire first insulating layer and base substrate, is processed using a CNC drill (step **85**).

[0016] Next, a first plating layer is formed on the first metal layer including inner walls of the blind via-hole and the through-hole (step **86**).

[0017] Next, a first circuit pattern layer is formed by patterning the first metal layer and the first plating layer (step **87**). At this time, the first metal layer and the first plating layer formed in the flexible domain F are removed.

[0018] Next, a second insulating layer is laminated on the rigid domain R, and a second metal layer is laminated on the second insulating layer including the flexible domain F (step **88**). At this time, like the above step **82**, it is preferred that the first insulating layer is made of a cured insulator so that the first insulating layer is not laminated on the flexible domain F.

[0019] Next, a via-hole is processed (step **89**). At this time, the via-hole is formed by processing the second insulating layer, which is exposed by a second window, with C02 laser after processing the second window by removing the second metal layer in a domain in which the via-hole is to be processed.

[0020] Next, a second plating layer is formed on the second metal layer including the via-hole (step **810**).

[0021] Next, a second circuit pattern layer is formed by patterning the second metal layer and the second plating layer (step **811**). At this time, like the step **87**, the second metal layer and the second plating layer formed in the flexible domain F are removed.

[0022] Finally, a third insulating layer is laminated on the rigid domain R, a third metal layer is laminated on the third insulating layer including the flexible domain F, and a third circuit pattern layer is formed (step **812**). That is, since this step, a step of forming a third build-up layer, is equal to a method of forming a first build-up layer or a second build-up layer, repeated description will be omitted.